



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 040679/0439

Applicant: Haruhiko MURATA

Title: IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD
HAVING SOLDER BUMPS

Serial No.: 08/825,400

Filed: March 28, 1997

Examiner: Norris, Jeremy C.

Art Unit: 2827

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56 and 37 CFR §1.97**

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO SB/08 is a list of documents known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 CFR 1.56. A copy of the listed document is being submitted to comply with the provisions of 37 CFR 1.97 and 1.98.

The submission of any documents herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a prima facie prior art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The instant Information Disclosure Statement is being filed after the mailing date of the final action under 37 C.F.R. §1.113. The IDS is also being filed under the provisions set forth in 37 C.F.R. 1.97(i), whereby the Information Disclosure Statement and listed references will be placed in the file at the PTO, but is not required to be considered. As prosecution is still pending, Applicants do request that the Examiner consider the references, and initial and return the attached PTO SB/08 form.

RELEVANCE OF EACH DOCUMENT

Document A1 relates to a fixture for forming component-mounting solder bumps on a circuit board.

Document A2 relates to forming a solder bump electrode on pads of an Integrated Circuit wafer, whereby a solder ball is fused on each pad with a hot plate.

Document A3 relates to a semiconductor chip that has an adhering layer cap, bump electrode, jig and spacer.

Document A4 relates a flip chip semiconductor device in which heights of ends of solder bumps are arranged to evaluate electrical characteristics of a chip.

Respectfully submitted,

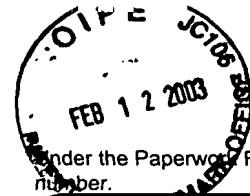
February 12, 2002
Date

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Substitute for form 1449B/PTO				<i>Complete if Known</i>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	08/825,400
Date Submitted: February 12, 2003				Filing Date	03/28/1997
(use as many sheets as necessary)				First Named Inventor	Haruhiko MURATA
Sheet	1	of	1	Group Art Unit	2827
				Examiner Name	J. Norris
				Attorney Docket Number	040679-0439

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST 3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

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⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, D.C. 20231.